Ultra Low-voltage Operation of Devices for Internet of Things (IOT) Applications

Low-power Electronics Association & Project (LEAP)

May 14, 2014

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Outline

1. Four Years’ Footprints of the Project
   ✓ Start of the project
   ✓ New device fabrication Scheme
   ✓ Recent topics on low-voltage devices

2. Prospective Applications of Ultra Low-voltage Devices

3. Toward the End of the Project

4. Summary
Five Themes in LEAP

- SOTB (SOI Transistor)
- Atom Switch Device
- Magnetic Resistance Change Device (MRAM)
- Phase-Change Device (PCM)
- 3D nano-Carbon

10 Companies
Five Themes in LEAP

Hierarchy of Computing

- Logic
- Cache Memory
- High-Speed Storage
- High-Density Storage

10 Companies

- SOTB (SOI Transistor)
- Atom Switch Device
- Magnetic Resistance Change Device (MRAM)
- Phase-Change Device (PCM)
- 3D nano-Carbon

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Five Themes in LEAP

- Logic
- Cache Memory
- High-Speed Storage
- High-Density Storage

Hierarchy of Computing:
- SOTB (SOI Transistor)
- Atom Switch Device
- Magnetic Resistance Change Device (MRAM)
- Phase-Change Device (PCM)
- 3D nano-Carbon

Server

Storage

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## Voltage Reduction Targets

<table>
<thead>
<tr>
<th>Time Span</th>
<th>Voltage</th>
<th>Logic</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Now</td>
<td>1.2-1.0V</td>
<td>CMOS</td>
<td>DRAM, SRAM</td>
</tr>
<tr>
<td>Short</td>
<td>&lt;0.8V</td>
<td>Fin-FET, FD-SOI</td>
<td>DRAM, SRAM</td>
</tr>
<tr>
<td>New Devices</td>
<td></td>
<td>SOTB</td>
<td>SRAM, MRAM, PCM</td>
</tr>
<tr>
<td>Medium &amp; Long</td>
<td>&lt;0.4V</td>
<td></td>
<td>Atom Switch</td>
</tr>
</tbody>
</table>

FD-SOI; Fully Depleted Silicon On Insulator

SOTB; Silicon ON Thin BOX

MRAM; Magnetic Random Access Memory

PCM; Phase Change Memory

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Why 0.4V?

Power consumption:

\[ P = CV_{dd}^2 f + I_{\text{leak}} V_{dd} \]

\(P\) = Active \(CV_{dd}^2 f\) + Leak \(I_{\text{leak}} V_{dd}\)

Power per operation:

\[ E = CV_{dd}^2 + I_{\text{leak}} V_{dd}/af \]

\(E\) = Active \(CV_{dd}^2\) + Leak \(I_{\text{leak}} V_{dd}/af\)

- \(a\): activation ratio

\[ E = CV_{dd}^2 f + I_{\text{leak}} V_{dd}/af \]

should be minimum

At around 0.4V, computing energy becomes minimum
Efficient Device Fabrication for R&D & Prototyping

CMOS fabrication at a production line followed by a new device fabrication in Tsukuba AIST’s line

- 300mm Production Line
- Cu
- Functional Module
- CMOS
- Tsukuba 300mm BEOL Line
- Atom Switch
- Local wiring (Immersion ArF)
- Semi-global wiring (KrF)
- Atom Switch
- Tukuba SCR300mm BEOL Line
- 65nmCMOS
- 300mm Volume Production Line
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# Footprints of the Project

<table>
<thead>
<tr>
<th>Financial Year</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atom Switch</td>
<td>Line Ramp-up</td>
<td>Single Device Verification</td>
<td>Integration Process Development</td>
<td>Macro-level Integration</td>
<td>Reliability-aware Integration</td>
</tr>
<tr>
<td></td>
<td>• CVD machine for Polymer Solid Electrolyte Deposition</td>
<td>• Development of 3-terminal Atom Switch</td>
<td>• Fabrication of AS on 65-nm CMOS</td>
<td>• 6x6 programmable logic verification</td>
<td>• 1/10 power @0.4V compared with that of 1.2 V</td>
</tr>
<tr>
<td></td>
<td>• PSE material selection</td>
<td>• Integration Process suitable for BEOL-PF</td>
<td>• 3x3 programmable logic verification</td>
<td></td>
<td>• 1/20 area compared with that of SRAM</td>
</tr>
</tbody>
</table>

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SOTB (Silicon on Thin BOX)

Hierarchy of Computing

- High-Density Storage
- High-Speed Storage
- Cache Memory
- Logic

SOTB (SOI Transistor)

Atom Switch Device

Magnetic Resistance Change Device (MRAM)

Phase-Change Device (PCM)

3D nano-Carbon

Server

Storage

High-speed Storage

High-density Storage

SSD NAND Flash

Logic

First Memory

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From Bulk to Thin and Lean Channel

FD-SOI; Fully Depleted SOI

FD-SOI; Fully Depleted SOI with Thin BOX
Origin of Thin BOX FD-SOI

“Limitations on MOS ULSIs”
M. Fukuma
Dig. Tech. Papers,

• Vth variability reduction due to intrinsic channel
• Suppression of SCE by back bias
First Report on SOTB

“Silicon on thin BOX: A new paradigm of the CMOSFET for low-power and high-performance application featuring wide-range back-bias control”,


Fig. 1 Schematic cross-sectional view and device concepts of a device with an ultra-thin box layer.
First Report on SOTB

“Silicon on thin BOX: A new paradigm of the CMOSFET for low-power and high-performance application featuring wide-range back-bias control”,


N. Sugii et al., IEDM, 2008.

CANON’s ELTRAN
Variability Reduction by SOTB

Raised Source & Drain (Selective Si epi)

SOI layer (Channel)

BOX

50nm

Cumulative probability

0 0.2 0.4 0.6 0.8

Vth(V)

SOTB

Bulk

Same worst leakage

Y. Yamamoto et al., Symp. VLSI Technology, JJ2-4, 2013

Y. Yamamoto et al., Symp. VLSI Technology, p. 109, 2012

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Extreme Low-voltage Operation of SRAM

“Ultralow-Voltage Operation of Silicon-on-Thin-BOX (SOTB) 2Mbit SRAM Down to 0.37 V Utilizing Adaptive Back Bias”

VLSI Technology, JJ2-4, 2013

![Image of SRAM chip]

![Image of SRAM comparison]

![Graph showing FailBit and VDD relationship]

- Measured data
- V_min = 0.37V

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32-bit RISC Processor by SOTB

- 32-bit RISC Processor was demonstrated to operate at as low as 0.4 V.
- Several interfaces are implemented taking sensor module applications into consideration.

Chip Photo

K. Ishibashi et. al., Cool Chips XVII, 2014

SRAM  CPU  UART interface

ROM interface  Timer  SPI interface

ROM  Clock  Sensor

embedded  Not embedded

SPI: Serial Peripheral Interface
UART: Universal Asynchronous Receiver Transmitter
Comparison of Energy Consumption

Collaboration with UEC, KIT, Keio U and Shibaura IT

Graph 1: Comparison of Max Frequency (MHz) and Voltage (Vdd) for SOTB and Bulk technologies. A 0.3V reduction results in a 22x reduction.

Graph 2: Comparison of Energy Consumption (E) and Voltage (Vdd) for SOTB and Bulk technologies. The 32nm CPU achieves 13.4 pJ at 0.35V.
Flex-Power FPGA

Each element is independently back-biased

Critical Path
Low-Vt
Fast but High Power

High-Vt
Low Power
but Slow

Vth is set high for non-critical pass MOSFET

Collaboration with AIST

N. Sugii, et al., S3S Conference 2013,
C. Ma, et al., Design Gaia 2013

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Atom Switch

Hierarchy of Computing

- Logic
- Cache Memory
- High-Speed Storage
- High-Density Storage

Atom Switch Device

- SOTB (SOI Transistor)
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Server

Storage

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What’s Atom Switch?

Resistance change switch using generation and dissolution of Cu bridge
Two-terminal Atom Switch

Atom Switch

M5
M4
M3
M2
M1

M5
M4

300nm
Three-terminal Atom Switch

Atom Switch

M5
M4
M3
M2
M1

Control

Terminal1
Terminal2

300nm
Results of Preliminary Experiments

ON (Bridge Formation)

OFF (Dissolution)

Read

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Basic Concept of Compact Switch over Logic

Advantages
- Switch array over logics
- Low power consumption
- Low $C_{\text{input}}$

Performance

<table>
<thead>
<tr>
<th></th>
<th>Conventional PLD</th>
<th>PLD by Atom Switch</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>[in operation]</strong> Charge and discharge energy consumed by wire</td>
<td>1</td>
<td>1/2</td>
</tr>
<tr>
<td><strong>[in stand-by]</strong> Stand-by power by switch</td>
<td>30mW</td>
<td>0</td>
</tr>
</tbody>
</table>

Sea of Switch
Switch Plane
Logic Plane

SRAM (Memory of ON/OFF)
Pass Transistor
Atom Switch

(Both for SRAM and Pass Tr)

Conventional PLD
PLD by Atom Switch

Atomic Switch

Charge and discharge energy consumed by wire

Stand-by power by switch

30mW

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Logic Cell Architecture

- Each logic block includes 2 LUTs with 4 inputs
- 368 three-terminal atom switches (CAS) are used

Miyamura et al., IEDM 2012, p. 247
Comparison between SRAM switch and Atom Switch

Logic Cell Area; -75%
Signal Delay; -65%
Operation Power; -61%

Logic Cell with SRAM Switch
- 65nm 1P7M CMOS
- Cell : 2x 4input LUT
- Switch : Multiplexer
- Logic : CoreTr

Logic Cell with Atom Switch
- 65nm 1P7M CMOS
- Cell : 2x 4 input LUT
- CAS : 368bit/Cell
- Logic : CoreTr
- Selector : HV18

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## Operation Speed

<table>
<thead>
<tr>
<th></th>
<th>SRAM Switch</th>
<th>Atom Switch</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>LFSR24 (24bit Linear Feedback Shift Register)</strong></td>
<td><img src="#" alt="Graph" /></td>
<td><img src="#" alt="Graph" /></td>
</tr>
<tr>
<td><strong>MPY4 (4bit Multiplier)</strong></td>
<td><img src="#" alt="Graph" /></td>
<td><img src="#" alt="Graph" /> <img src="#" alt="0.30V, 150kHz" /></td>
</tr>
</tbody>
</table>

**SRAM Switch**
- **FAIL**
- **PASS**

**Atom Switch**
- **0.30V, 150kHz**

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MRAM and PCM

Hierarchy of Computing

- Logic
- Cache Memory
- High-Speed Storage
- High-Density Storage

SOTB (SOI Transistor)
Atom Switch Device
Magnetic Resistance Change Device (MRAM)
Phase-Change Device (PCM)
3D nano-Carbon

Server
Storage
SSD
NAND

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MTJ Fabricated between Cu Layers

Spin Transfer Torque MRAM

Current

MTJ*

Pinned layer
Tunneling insulator
Free layer

Cu Inter-
connect

Drain
Source

MOSFET

(*MTJ: Magnetic Tunnel Junction)

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TRAM (topological switching random access memory)

Non-melting and low-power resistance change of super-lattice

- **Conventional GeSbTe alloy**
  Phase change by Joule heating

  - SET (crystal)
  - RESET (amorphous)

  Melting & Rapid cooling

- **GeTe/Sb$_2$Te$_3$ super-lattice** concept proposed by J. Tominaga
  Resistance change by charge injection

  - Resistance change
    - Low-resistance
    - High-resistance
  - Melting is not needed

- **Ge atomic movement**

  TEM after 1M cycles

  S. Kato et al., SSDM2013

  N. Takaura et al., VLSI2013

  T. Ohyanagi et al., IEDM2013

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Prospective Applications of Ultra Low-voltage Devices

- Automobile
- Server
- Data Center
- Internet of Things
- Cloud Computing
- Resilient Country
- Watching
- Medical Care
- Health Care
- Agriculture
- Energy Management System
- Environment & Energy
- Safe & Secure
- Low birthrate & Aging Society
- Nursing Care
- Green of IT
- Sensing
- Information Processing
- Information Storage
- Ubiquitous Sensor Network
- Smart Phone
- Network Connection

- Logic
- 1st Memory
- High Speed Storage
- Volume Storage
- Hierarchy of Computing
- SOTB
- Atom Switch
- MRAM
- PCM
- Carbon Interconnect

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Toward the End of the Project

CMOS fabrication at a production line followed by the BEOL device fabrication in Tsukuba

Functional Module

CMOS

300mm Production Line

Cu

300mm BEOL Line

Tsukuba

Open Innovation

Input of Design Platform

Verification of New LSIs Using LEAP’s New Devices

System, Equipment Manufacturer

LSI Vendor

University

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Ultra-low Power Device Forum

CMOS fabrication at a production line followed by the BEOL device fabrication in Tsukuba

300mm Production Line

Functional Module

Cu

Cu

Tsukuba 300mm BEOL Line

Forum on Application of Ultra Low-power Integrated Circuits

Input of Design Platform

System, Equipment Manufacturer

LSI Vendor

University

Verification of New LSIs Using LEAP’s New Devices

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Summary

• A production line and the Tsukuba 300-mm SCR was combined to promote the integration of new devices.
• Unified integration process was proved to be efficient for experimental device fabrication and prototyping.
• Low voltage operation of devices were demonstrated not by a single device but by an integrated chip.
• IOT is surely the most suitable field for the application of our new devices.
Acknowledgements

This work was performed as "Ultra-Low Voltage Device Project" funded and supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy and Industrial Technology Development Organization (NEDO).

A part of the device processing was operated by the SCR Management Office, the National Institute of Advanced Industrial Science and Technology (AIST).